EP300-Series EPLDs
High-Performance
8-Macrocell Devices

Data Sheet

Features

- Low-power, direct replacement for GAL 16V8 and most 20-pin PAL devices
- 8 macrocells with configurable I/O architecture, allowing up to 18 inputs and 8 outputs
- High speed (EP330 tPD = 12 ns)
- EP320 offers "zero power" (typically 10 µA standby)
- 100% generically testable to provide 100% programming yield
- Available in 20-pin windowed ceramic DIP, and plastic DIP, J-lead, and SOIC packages
- A+PLUS software support featuring schematic capture, Boolean equation, state machine, truth table, and netlist design entry methods
- Extensive third-party software and programming support

General Description

Altera's EP300-series Erasable Programmable Logic Devices (EPLDs) provides a high-speed, low-power pin-compatible replacement for 20-pin programmable logic devices such as PALs and GALs. EP300-series EPLDs are available in 20-pin windowed ceramic DIP, and plastic one-time-programmable (OTP) DIP, J-lead (PLCC), and SOIC packages. See Figure 1.

Figure 1. Package Pin-Out Diagrams

Package outlines not drawn to scale.

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<table>
<thead>
<tr>
<th>DIP</th>
<th>J-Lead</th>
<th>SOIC</th>
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<td>Ceramic/Plastic</td>
<td>Plastic</td>
<td>Plastic</td>
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Features

- High-performance 8-macrocell EPLD
  - Combinatorial speeds with $t_{PD} = 30$ ns
  - Counter frequencies up to 28.6 MHz
  - Pipelined data rates up to 45.5 MHz
- Very low power
  - $I_{CC} = 3$ mA (typical) for an 8-bit counter at 1 MHz
  - $I_{CC} = 10$ µA (typical) in standby mode
- Available in 20-pin windowed ceramic and plastic, one-time-programmable dual in-line packages (DIPs)
- Macrocell flip-flops can be individually programmed for registered or combinatorial operation

Figure 10 shows pin-outs for the EP320 EPLD.

Figure 10. EP320 Pin-Out Diagram

Package outline not drawn to scale.