Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Power Standby ............... 50µW Max
- Low Power Operation .............. 20mW/MHz Max
- Fast Access Time .................. 200ns Max
- Data Retention ..................... at 2.0V Min
- TTL Compatible Input/Output
- High Output Drive - 1 TTL Load
- On-Chip Address Registers
- Common Data In/Out
- Three-State Output
- Easy Microprocessor Interfacing

Description

The HM-6561/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>TEMPERATURE RANGE</th>
<th>220ns</th>
<th>300ns</th>
<th>PKG. NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CERDIP</td>
<td>-55°C to +125°C</td>
<td>HM1-6561B/883</td>
<td>HM1-6561/883</td>
<td>F18.3</td>
</tr>
</tbody>
</table>

Pinout

HM-6561/883 (CERDIP)

TOP VIEW

- A3 1
- A2 2
- A1 3
- A0 4
- A5 5
- A6 6
- A7 7
- GND 8
- E 9
- VCC 10
- A4 11
- W 12
- ST 13
- DQ3 14
- DQ2 15
- DQ1 16
- DQ0 17
- SS 18

<table>
<thead>
<tr>
<th>PIN</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Address Input</td>
</tr>
<tr>
<td>E</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>W</td>
<td>Write Enable</td>
</tr>
<tr>
<td>S</td>
<td>Chip Select</td>
</tr>
<tr>
<td>DQ</td>
<td>Data In/Out</td>
</tr>
</tbody>
</table>

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
NOTES:
1. All lines positive logic-active high.
2. Three-state Buffers: A high → output active.
3. Data Latches: L high → Q = D and Q latches on falling edge of L.
4. Address Latches and Gated Decoders: Latch on falling edge of E and gate on falling edge of E.
Absolute Maximum Ratings

- **Supply Voltage**: +7.0V
- **Input or Output Voltage**: GND -0.3V to VCC +0.3V
- **ESD Classification**: Class 1

Thermal Information

- **Thermal Resistance**
  - $\theta_{JA}$
  - $\theta_{JC}$

- **CERDIP Package**: $74^\circ$C/W, $18^\circ$C/W
- **Maximum Storage Temperature Range**: -65°C to +150°C
- **Maximum Junction Temperature**: +175°C
- **Maximum Lead Temperature (Soldering 10s)**: +300°C

Die Characteristics

- **Gate Count**: 1944 Gates

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

- **Operating Voltage Range**: +4.5V to +5.5V
- **Operating Temperature Range**: -55°C to +125°C
- **Input Low Voltage**: 0V to +0.8V
- **Input High Voltage**: VCC - 2.0V to VCC
- **Input Rise and Fall Time**: 40ns Max

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>(NOTE 1) CONDITIONS</th>
<th>GROUP A SUBGROUPS</th>
<th>TEMPERATURE</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Low Voltage</td>
<td>VOL</td>
<td>VCC = 4.5V, IOL = 1.6mA</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-</td>
<td>0.4</td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>VOH</td>
<td>VCC = 4.5V, IOH = -0.4mA</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>2.4</td>
<td>-</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>II</td>
<td>VCC = 5.5V, VI = GND or VCC</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>Input/Output Leakage Current</td>
<td>IIOZ</td>
<td>VCC = 5.5V, VIO = GND or VCC</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>Data Retention Supply Current</td>
<td>ICCDR</td>
<td>VCC = 2.0V, E = VCC, IO = 0mA</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td>Operating Supply Current</td>
<td>ICCOP</td>
<td>VCC = 5.5V, (Note 2), E = 1MHz, W = GND, VI = VCC or GND</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>Standby Supply Current</td>
<td>ICCSB</td>
<td>VCC = 5.5V, IO = 0mA, VI = VCC or GND</td>
<td>1, 2, 3</td>
<td>$-55^\circ$C $\leq T_A \leq +125^\circ$C</td>
<td>-</td>
<td>10</td>
</tr>
</tbody>
</table>

NOTES:
1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.
TABLE 2. HM-6561/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>(NOTES 1, 2) CONDITIONS</th>
<th>GROUP A SUB-GROUPS</th>
<th>TEMPERATURE</th>
<th>LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>HM-6561B/883</td>
</tr>
<tr>
<td>Chip Enable Access Time</td>
<td>(1) TELQV</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>- 220 - 300 ns</td>
</tr>
<tr>
<td>Address Access Time</td>
<td>(2) TAVQV</td>
<td>VCC = 4.5 and 5.5V (Note 3)</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>- 220 - 300 ns</td>
</tr>
<tr>
<td>Chip Select Output Enable Time</td>
<td>(3) TSLQX</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>5 - 5 ns</td>
</tr>
<tr>
<td>Chip Select Output Disable Time</td>
<td>(4) TSHQZ</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>- 120 - 150 ns</td>
</tr>
<tr>
<td>Chip Enable Pulse Negative Width</td>
<td>(5) TELEH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>220 - 300 ns</td>
</tr>
<tr>
<td>Chip Enable Pulse Positive Width</td>
<td>(6) TEHEL</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>100 - 100 ns</td>
</tr>
<tr>
<td>Address Setup Time</td>
<td>(7) TAVEL</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>0 - 0 ns</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>(8) TELAX</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>40 - 50 ns</td>
</tr>
<tr>
<td>Data Setup Time</td>
<td>(9) TDVWH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>100 - 150 ns</td>
</tr>
<tr>
<td>Data Hold Time</td>
<td>(10) TWHDX</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>0 - 0 ns</td>
</tr>
<tr>
<td>Write Data Delay Time</td>
<td>(11) TWLDV</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>20 - 30 ns</td>
</tr>
<tr>
<td>Chip Select Write Pulse Setup Time</td>
<td>(12) TWLSH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>120 - 180 ns</td>
</tr>
<tr>
<td>Chip Enable Write Pulse Setup Time</td>
<td>(13) TWLEH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>120 - 180 ns</td>
</tr>
<tr>
<td>Chip Select Write Pulse Hold Time</td>
<td>(14) TSLWH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>120 - 180 ns</td>
</tr>
<tr>
<td>Chip Enable Write Pulse Hold Time</td>
<td>(15) TELWH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>120 - 180 ns</td>
</tr>
<tr>
<td>Write Enable Pulse Width</td>
<td>(16) TWLWH</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>120 - 180 ns</td>
</tr>
<tr>
<td>Read or Write Cycle Time</td>
<td>(17) TELEL</td>
<td>VCC = 4.5 and 5.5V</td>
<td>9, 10, 11</td>
<td>-55°C ≤ TA ≤ +125°C</td>
<td>320 - 400 ns</td>
</tr>
</tbody>
</table>

NOTES:
1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: $I_{OL} = 1.6\text{mA}$, $I_{OH} = -0.4\text{mA}$, $CL = 50\text{pF}$ (min) - for $CL$ greater than 50pF, access time is derated by 0.15ns per pF.
3. $TAVQV = TELQV + TAVEL$. 

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**HM-6561/883**
NOTE:
1. Test head capacitance includes stray and jig capacitance.

**TABLE 3. HM-6561/883 ELECTRICAL PERFORMANCE SPECIFICATIONS**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>NOTE</th>
<th>TEMPERATURE</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>VCC = Open, f = 1MHz, All Measurements</td>
<td>1</td>
<td>$T_A = +25^\circ C$</td>
<td>-</td>
<td>8 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Referenced to Device Ground</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>VCC = Open, f = 1MHz, All Measurements</td>
<td>1</td>
<td>$T_A = +25^\circ C$</td>
<td>-</td>
<td>10 pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Referenced to Device Ground</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

**TABLE 4. APPLICABLE SUBGROUPS**

<table>
<thead>
<tr>
<th>CONFORMANCE GROUPS</th>
<th>METHOD</th>
<th>SUBGROUPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Test</td>
<td>100%/5004</td>
<td></td>
</tr>
<tr>
<td>Interim Test</td>
<td>100%/5004</td>
<td>1, 7, 9</td>
</tr>
<tr>
<td>PDA</td>
<td>100%/5004</td>
<td>1</td>
</tr>
<tr>
<td>Final Test</td>
<td>100%/5004</td>
<td>2, 3, 8A, 8B, 10, 11</td>
</tr>
<tr>
<td>Group A</td>
<td>Samples/5005</td>
<td>1, 2, 3, 7, 8A, 8B, 9, 10, 11</td>
</tr>
<tr>
<td>Groups C &amp; D</td>
<td>Samples/5005</td>
<td>1, 7, 9</td>
</tr>
</tbody>
</table>

**Test Load Circuit**

NOTE:
1. Test head capacitance includes stray and jig capacitance.
The HM-6561/883 Read Cycle is initiated on the falling edge of \( E \). This signal latches the input address word into on-chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data, \( S_1 \) and \( S_2 \) must be low and \( W \) must be high. The output data will be valid at access time (TELQV).

The HM-6561/883 has output data latches that are controlled by \( E \). On the rising edge of \( E \) the present data is latched and remains latched until \( E \) falls. Either or both \( S_1 \) or \( S_2 \) may be used to force the output buffers into a high impedance state.
The write cycle begins with the $E$ falling edge latching the address. The write portion of the cycle is defined by $E$, $S1$, $S2$, and $W$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $E$, $S1$, $S2$, or $W$. The data setup and data hold times ($TDVWH$ and $TWHDX$) must be referenced to the terminating signal. For example, if $S2$ rises first, data setup and hold times become $TDVS2H$ and $TS2HDX$; and are numerically equal to $TDVWH$ and $TWHDX$.

Data input/output multiplexing is controlled by $W$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following examples illustrate the timing required to avoid bus conflicts.

**Case 1:** Both $S1$ and $S2$ Fall Before $W$ Falls.
If both selects fall before $W$ falls, the RAM outputs will become enabled. $W$ is used to disable the outputs, so a disable time ($TWLQ = TWLDV$) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because $TWLDV + TDVWH$ is greater than $TWLWH$. In this case $TWLSL + TSHWH$ are meaningless and can be ignored.

**Case 2:** $W$ Falls Before Both $S1$ and $S2$ Fall.
If one or both selects are high until $W$ falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and $TWLDV$ is ignored. Since $W$ is not used to disable the outputs it can be shorter than in Case 1; $TWLWH$...
is the minimum write pulse. At the end of the write period, if \( W \) rises before either select the outputs will enable reading data just written. They will not disable until either select goes high (TSHQZ).

If a series of consecutive write cycles are to be performed, \( W \) may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact data may be modified as many times as desired with \( E \) remaining low.

### Burn-In Circuit

<table>
<thead>
<tr>
<th>CASE 1</th>
<th>IF</th>
<th>OBSERVE</th>
<th>IGNORE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Both ST and S2 = Low Before ( W ) = Low</td>
<td>TWLOZ TWLDV TDVWH</td>
<td>TWLWH</td>
<td></td>
</tr>
</tbody>
</table>

| CASE 2          | \( W \) = Low Before Both ST and S2 = Low | TWLWH    | TWLOZ TWLDV |

**NOTES:**
- All resistors 47k\( \Omega \) ±5%.
- \( F0 = 100\text{kHz} \) ±10%.
- \( F1 = F0 \div 2, F2 = F1 \div 2, F3 = F2 \div 2 \ldots F12 = F11 \div 2 \).
- \( VCC = 5.5V \pm 0.5V \).
- \( VIH = 4.5V \pm 10\% \).
- \( VIL = -0.2V \) to +0.4V.
- \( C1 = 0.01\mu F \) Min.
**Die Characteristics**

**DIE DIMENSIONS:**
132 x 160 x 19 ±1mils

**WORST CASE CURRENT DENSITY:**
1.337 x 10^5 A/cm^2

**LEAD TEMPERATURE (10s soldering):**
≤ 300°C

**METALLIZATION:**
- Type: Si - Al
- Thickness: 11k Å ±2k Å

**GLASSIVATION:**
- Type: SiO_2
- Thickness: 8k Å ±1k Å

**Worst Case Current Density:**
1.337 x 10^5 A/cm^2

**Metallization Mask Layout**

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