ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE858M
NTE858SM
Integrated Circuit
Dual, Low–Noise JFET–Input Operational Amplifier

Description:

The NTE858M and NTE858SM are dual, low–noise JFET input operational amplifiers combining two state–of–the–art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, these devices exhibit low–noise and low harmonic distortion making them ideal for use in high–fidelity audio amplifier applications.

Features:

- Available in Two Different Package Types:
  8–Lead Mini DIP (NTE858M)
  SOIC–8 Surface Mount (NTE858SM)
- Low Input Noise Voltage: 18nV$\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: $10^{12}\Omega$ Typ
- High Slew Rate: 13V/µs Typ
- Wide Gain Bandwidth: 4MHz Typ
- Low Supply Current: 1.4mA per Amp

Absolute Maximum Ratings:

Supply Voltage
V_{CC} . . . . +18V
V_{EE} . . . . –18V
Differential Input Voltage, V_{ID} . . . . ±30V
Input Voltage Range (Note 1), V_{IDR} . . . . ±15V
Output Short–Circuit Duration (Note 2), t_S . . . . Continuous
Power Dissipation, P_D 680mW
Derate Above T_A = +47°C . . . . 10mW/°C
Operating Ambient Temperature Range, T_A . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . –65° to +150°C

Note 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15V, whichever is less.

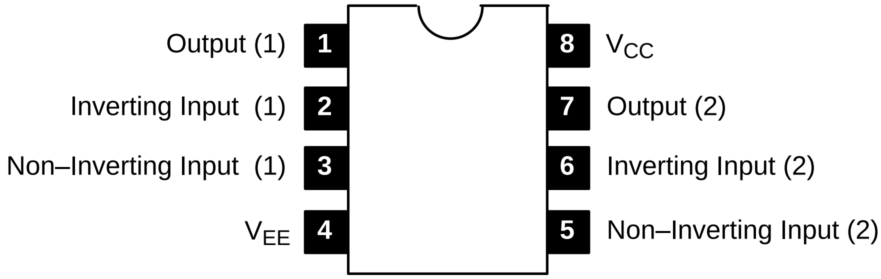
Note 2. The output may be shorted to GND or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratungs are not exceeded.

Electrical Characteristics: (V_{CC} = +15V, V_{EE} = –15V, T_A = +25°C unless otherwise specified)

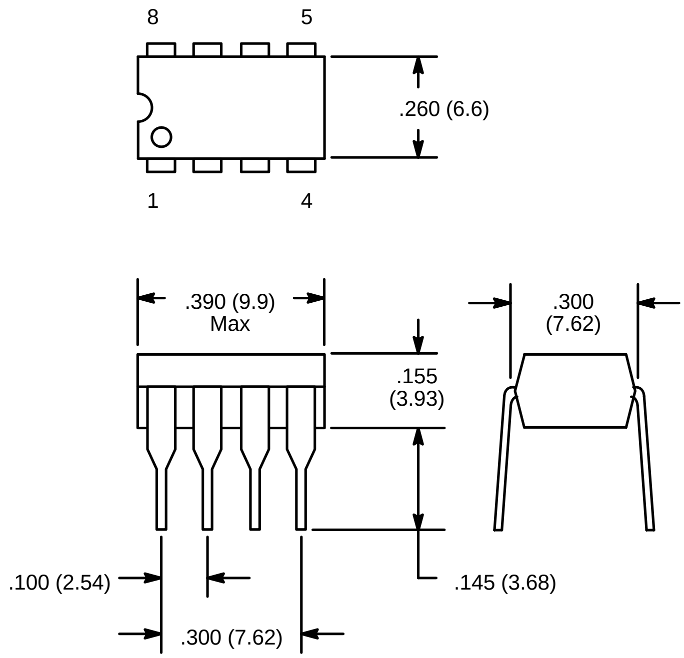
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 10k$, $V_{CM} = 0$		–	3	10	mV
			T_A = 0 to +70°C	–	–	13	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	T_A = 0 to +70°C		–	10	–	μV/°C
Input Offset Current	I_{IO}	$V_{CM} = 0$, Note 3		–	5	50	pA
			T_A = 0 to +70°C	–	–	2	nA
Input Bias Current	I_{IB}	$V_{CM} = 0$, Note 3		–	30	200	pA
			T_A = 0 to +70°C	–	–	7	nA
Input Resistance	r_i			–	10^{12}	–	Ω
Common Mode Input Voltage Range	V_{ICR}			±10	+15, –12	–	V
Large–Signal Voltage Gain	A_{VOL}	$V_O = \pm 10V$, $R_L \leq 2k$		25	150	–	V/mV
			T_A = 0 to +70°C	15	–	–	V/mV
Output Voltage Swing (Peak–to–Peak)	V_O	$R_L = 10k$		24	28	–	V
		$R_L \geq 10k$	T_A = 0 to +70°C	24	–	–	V
		$R_L \geq 2k$		20	–	–	V
Common Mode Rejection Ratio	CMRR	$R_S \leq 10k$		70	100	–	dB
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10k$		70	100	–	dB
Supply Current (Each Amplifier)	I_D			–	1.4	2.5	mA
Unity Gain Bandwidth	BW			–	4	–	MHz
Slew Rate	SR	$V_{IN} = 10V$, $R_L = 2k$, $C_L = 100pF$		–	13	–	V/μs
Rise Time	t_r			–	0.1	–	μs
Overshoot Factor		$V_{IN} = 20mV$, $R_L = 2k$, $C_L = 100pF$		–	10	–	%
Equivalent Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 1000Hz		–	18	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current	i_n	$R_S = 100\Omega$, f = 1000Hz		–	0.01	–	$pA/\sqrt{Hz}$
Total Harmonic Distortion	THD	$V_{O(RMS)} = 10V$, $R_S \leq 1k$, $R_L \geq 2k$, f = 1000Hz		–	0.01	–	%
Channel Separation		$A_V = 100$		–	120	–	dB

Note 3. Input Bias currents of JFET input operational amplifiers approximately double for every 10°C rise in Junction Temperature. To maintain Junction Temperature as close to Ambient Temperature as possible, pulse techniques must be used during test.

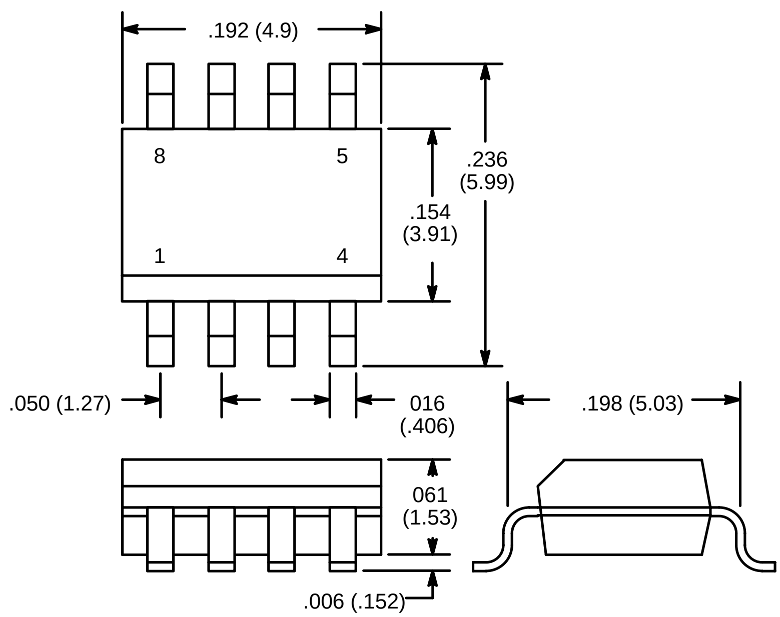
Pin Connection Diagram



NTE858M



NTE858SM



NOTE: Pin1 on Beveled Edge

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.