• High-Performance Operation:
  - $f_{\text{max}}$ (no feedback)
    - TIBPAL20L8' . . . 71.4 MHz
  - $f_{\text{max}}$ (Internal feedback)
    - TIBPAL20R' . . . 58.8 MHz
  - $f_{\text{max}}$ (external feedback)
    - TIBPAL20R' . . . 55.5 MHz
  - Propagation Delay
    - TIBPAL20' . . . 10 ns Max

• Functionally Equivalent, but Faster Than Existing 24-Pin PLD Circuits

• Preload Capability on Output Registers
  Simplifies Testing

• Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)

• Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs

• Security Fuse Prevents Duplication

• Dependable Texas Instruments Quality and Reliability

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>I INPUTS</th>
<th>3-STATE Q OUTPUTS</th>
<th>REGISTERED Q OUTPUTS</th>
<th>I/O PORTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAL20L8</td>
<td>14</td>
<td>2</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>PAL20R4</td>
<td>12</td>
<td>0</td>
<td>4 (3-state buffers)</td>
<td>4</td>
</tr>
<tr>
<td>PAL20R6</td>
<td>12</td>
<td>0</td>
<td>6 (3-state buffers)</td>
<td>2</td>
</tr>
<tr>
<td>PAL20R8</td>
<td>12</td>
<td>0</td>
<td>6 (3-state buffers)</td>
<td>0</td>
</tr>
</tbody>
</table>

**description**

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

All of the register outputs are set to a low level during power up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C.
functional block diagrams (positive logic)

TIBPAL20L8'

TIBPAL20R4'

\( \sim \) denotes fused inputs
functional block diagrams (positive logic)

TIBPAL20R6'

OE
CLK

EN 2
> C1

&
40 X 64

≥1
I = 0 2V
1D

Q
Q
Q
Q
Q
Q
Q
Q
I/O
I/O

TIBPAL20R8'

OE
CLK

EN 2
> C1

&
40 X 64

≥1
I = 0 2V
1D

Q
Q
Q
Q
Q
Q
Q
Q
I/O
I/O

≈ denotes fused inputs

Texas Instruments
logic diagram (positive logic)

Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.
logic diagram (positive logic)

Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.
logic diagram (positive logic)

Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .......................................................... 7 V
Input voltage (see Note 1) ................................................................. 5.5 V
Voltage applied to disabled output (see Note 1) ................................. 5.5 V
Operating free-air temperature range ........................................... 0°C to 75°C
Storage temperature range ......................................................... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Supply voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$ High-level input voltage</td>
<td>2</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$ Low-level input voltage</td>
<td>0.8</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$ High-level output current</td>
<td>−3.2</td>
<td>−3.2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{OL}$ Low-level output current</td>
<td>24</td>
<td>24</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$f_{clock}$ Clock frequency</td>
<td>0</td>
<td>71.4</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>$t_{W}$ Pulse duration, clock (see Note 2)</td>
<td>High</td>
<td>7</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{	ext{setup}}$ Setup time, input or feedback before clock$^\dagger$</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_{h}$ Hold time, input or feedback after clock$^\dagger$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$T_{A}$ Operating free-air temperature</td>
<td>0</td>
<td>25</td>
<td>75</td>
<td>°C</td>
</tr>
</tbody>
</table>

$^\dagger$ $f_{clock}$, $t_{W}$, $t_{	ext{setup}}$, and $t_{h}$ do not apply for TIBPAL20L8.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.
## Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>$V_{CC} = 4.75 \text{ V}$, $I_I = -18 \text{ mA}$</td>
<td>$-0.8$</td>
<td>$-1.5$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>$V_{CC} = 4.75 \text{ V}$, $I_O = 24 \text{ mA}$</td>
<td>$0.3$</td>
<td>$0.5$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$IOZH$†</td>
<td>$O_{Q}$ outputs, $I/O$ ports</td>
<td>$-20$</td>
<td></td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$IOZL$†</td>
<td>$O_{Q}$ outputs, $I/O$ ports</td>
<td>$-100$</td>
<td></td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_I$</td>
<td>$V_{CC} = 5.25 \text{ V}$, $V_I = 5.5 \text{ V}$</td>
<td>$0.2$</td>
<td></td>
<td>$\text{mA}$</td>
<td></td>
</tr>
<tr>
<td>$I_{HI}$†</td>
<td>$V_{CC} = 5.25 \text{ V}$, $V_I = 2.7 \text{ V}$</td>
<td>$-0.25$</td>
<td></td>
<td>$\text{mA}$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$‡</td>
<td>$V_{CC} = 5.25 \text{ V}$, $V_I = 0.4 \text{ V}$</td>
<td>$-30$</td>
<td>$-70$</td>
<td>$-130$</td>
<td>$\text{mA}$</td>
</tr>
<tr>
<td>$IOS$§</td>
<td>$V_{CC} = 5.25 \text{ V}$, $V_O = 0.5 \text{ V}$</td>
<td>$210$</td>
<td></td>
<td>$\text{mA}$</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC} = 5.25 \text{ V}$, $V_I = 0$, $OE = V_{IH}$</td>
<td></td>
<td></td>
<td>$\text{mA}$</td>
<td></td>
</tr>
<tr>
<td>$C_I$</td>
<td>$f = 1 \text{ MHz}$, $V_I = 2 \text{ V}$</td>
<td>$7$</td>
<td></td>
<td>$\text{pF}$</td>
<td></td>
</tr>
<tr>
<td>$C_O$</td>
<td>$f = 1 \text{ MHz}$, $V_O = 2 \text{ V}$</td>
<td>$8$</td>
<td></td>
<td>$\text{pF}$</td>
<td></td>
</tr>
<tr>
<td>$C_{CLK}$</td>
<td>$f = 1 \text{ MHz}$, $V_{CLK} = 2 \text{ V}$</td>
<td>$12$</td>
<td></td>
<td>$\text{pF}$</td>
<td></td>
</tr>
</tbody>
</table>

## Switching Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-Air Temperature (Unless Otherwise Noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITION</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{max}}$†</td>
<td>without feedback</td>
<td>with internal feedback (counter configuration)</td>
<td>$R_1 = 200 \Omega$, $R_2 = 390 \Omega$, See Figure 6</td>
<td>$71.4$</td>
<td>$58.8$</td>
<td>$55.5$</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>$I$, $I/O$</td>
<td>$O$, $I/O$</td>
<td></td>
<td>$3$</td>
<td>$8$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd}$</td>
<td>$CLK$</td>
<td>$Q$</td>
<td></td>
<td>$3$</td>
<td>$8$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{pd}$‡</td>
<td>$CLK$</td>
<td>Feedback input</td>
<td></td>
<td>$2$</td>
<td>$6$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>$OE$</td>
<td>$Q$</td>
<td></td>
<td>$2$</td>
<td>$6$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>$I$, $I/O$</td>
<td>$Q$</td>
<td></td>
<td>$2$</td>
<td>$6$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dia}$</td>
<td>$OE$</td>
<td>$I$, $I/O$</td>
<td></td>
<td>$3$</td>
<td>$8$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dia}$</td>
<td>$I$, $I/O$</td>
<td>$O$, $I/O$</td>
<td></td>
<td>$2$</td>
<td>$8$</td>
<td>$10$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{sk(ii)}$‖</td>
<td>Skew between registered outputs</td>
<td></td>
<td></td>
<td>$0.5$</td>
<td></td>
<td>$\text{ns}$</td>
<td></td>
</tr>
</tbody>
</table>

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.
‡ $I/O$ leakage is the worst case of $IOZH$ and $I_{IL}$ or $I_{IH}$ and $I_I$ respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. $V_O$ is set at 0.5 V to avoid test problems caused by test equipment ground degradation.
¶ See section for $f_{\text{max}}$ specifications. $f_{\text{max}}$ does not apply for TIBPAL20L8.
# This parameter applies to TIBPAL20R4 and TIBPAL20R6 only (see Figure 4 for illustration) and is calculated from the measured $f_{\text{max}}$ with internal feedback in the counter configuration.
‖ This parameter is the measurement of the difference between the fastest and slowest $t_{pd}$ (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.
programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5866.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With \( V_{CC} \) at 5 volts and Pin 1 at \( V_{IL} \), raise Pin 13 to \( V_{IH} \).
Step 2. Apply either \( V_{IL} \) or \( V_{IH} \) to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to \( V_{IL} \). Preload can be verified by observing the voltage level at the output pin.

![Figure 1. Preload Waveforms](image)

**NOTE 3:** \( t_d = t_{su} = t_h = 100 \text{ ns to } 1000 \text{ ns} \) \( V_{IHH} = 10.25 \text{ V to } 10.75 \text{ V} \)
power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of \( V_{CC} \) be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

\[ V_{CC} \quad 4 \text{ V} \quad t_{pd} \uparrow \quad 5 \text{ V} \]

\[ \text{Active Low} \]

\[ \text{Registered Output} \]

\[ V_{OH} \quad 1.5 \text{ V} \quad t_{SU} \uparrow \quad V_{OL} \]

\[ V_{IH} \quad 1.5 \text{ V} \quad 1.5 \text{ V} \quad t_{W} \quad V_{IL} \]

\( \uparrow \) This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

\( \uparrow \) This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms
**f\textsubscript{\text{max}} Specifications**

**f\textsubscript{\text{max}} without feedback, see Figure 3**

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time (t\text{su} + t\text{h}). However, the minimum f\textsubscript{\text{max}} is determined by the minimum clock period (t\text{w high} + t\text{w low}).

Thus, \( f\text{\textsubscript{\text{max}} without feedback} = \frac{1}{(t\text{w high} + t\text{w low})} \) or \( \frac{1}{(t\text{su} + t\text{h})} \).

![Figure 3. f\textsubscript{\text{max}} Without Feedback](image)

**f\textsubscript{\text{max}} with internal feedback, see Figure 4**

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, \( f\text{\textsubscript{\text{max}} with internal feedback} = \frac{1}{(t\text{su} + t\text{pd CLK-to-FB})} \).

Where \( t\text{pd CLK-to-FB} \) is the deduced value of the delay from CLK to the input of the logic array.

![Figure 4. f\textsubscript{\text{max}} With Internal Feedback](image)
$f_{\text{max}}$ SPECIFICATIONS

$f_{\text{max}}$ with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_{su} + t_{pd}$ CLK-to-Q).

Thus, $f_{\text{max}}$ with external feedback = \[ \frac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}. \]

Figure 5. $f_{\text{max}}$ With External Feedback
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Input

In-Phase Output

Out-of-Phase Output (see Note D)

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Notes:

A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_{r} = t_{f} ≤ 2 ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms
TYPICAL CHARACTERISTICS

POWER DISSIPATION

vs

FREQUENCY

8-BIT COUNTER MODE

Figure 11

PROPAGATION DELAY TIME†

vs

NUMBER OF OUTPUTS SWITCHING

Figure 12

PROPAGATION DELAY TIME

vs

NUMBER OF OUTPUTS SWITCHING

Figure 13

†Outputs switching in the same direction (tPLH compared to tPLH/tPHL to tPHL)